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4. A semiconductor device according to claim 2,
further comprising:

5. A semiconductor device comprising:

~~a first insulating film for covering the transistor;~~

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a second insulating film formed on the capacitor;

a local interconnection formed on the second insulating film, for electrically connecting the upper electrode of the capacitor to the first impurity region;

20 a third insulating film formed on the local
interconnection and the second insulating film;

a first wiring formed on the third insulating film and electrically connected to the second impurity region via a hole which is formed on the first insulating film, the second insulating film, and the third insulating film;

a fourth insulating film formed on the first

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second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

5 a first insulating film for covering the transistor;

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10 a capacitor formed on the first insulating film, the capacitor having a dielectric film formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film covering the capacitor; and

wherein a surface of the second insulating film is planarized and plasma annealed.

15 13. A method of manufacturing a semiconductor device comprising the steps of:

forming a transistor on a semiconductor substrate;

20 forming a first insulating film on the semiconductor substrate to cover the transistor;

forming a capacitor, which includes a dielectric film formed of either a ferroelectric material or a high- dielectric material and an upper electrode and a lower electrode formed to put the dielectric film therebetween, on the first insulating film;

forming a second insulating film over the capacitor;

planarizing an upper surface by polishing the second insulating film; and

applying a dehydration process to the second insulating film by plasma annealing.

5 14. A method according to claim 13, wherein the plasma annealing is performed by plasmanizing a single gas of one of N_2O , N_2 , NO , and O_2 , or a mixed gas including one of N_2O , N_2 , NO and O_2 .

10 15. A method of manufacturing a semiconductor device according to claim 13, wherein the second insulating film is formed by a plasma enhanced CVD method using a TEOS gas.

15 16. A method of manufacturing a semiconductor device according to claim 13, wherein cavity is formed in the second insulating film.

17. A method of manufacturing a semiconductor device according to claim 16, wherein upper portions of the cavity is exposed by polishing the second insulating film.

20 18. A method of manufacturing a semiconductor device according to claim 13, further comprising the step of:

forming a third insulating film on the second insulating film after the dehydration process.

25 19. A method of manufacturing a semiconductor device according to claim 13, further comprising the step of:

forming a fourth insulating film between the capacitor and the second insulating film to cover the capacitor; and

5 forming a wiring between the second insulating film and the fourth insulating film.

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